Application Note 342
T1/E1 Framer Initialization and Programming

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INTRODUCTION

This application note shows how to initialize and program Dallas T1/E1 framers. The DS2155, DS21Q55, and DS2156 do not require any special initialization after power-up, since they automatically initialize themselves by clearing and setting the proper registers.

This application note applies to the following products:

DS2141	DS21Q41	DS21Q42	DS2143
DS21Q43	DS21Q44	DS2151	DS2152
DS2153	DS2154	DS21FF42	DS21FT42
DS21FF44	DS21FT44	DS21352	DS21354
DS21552	DS21554	DS2155	DS21Q55
DS2156			

GENERAL INITIALIZATION

After power-up, when supplies and clocks have stabilized, internal registers must be initialized. Please note the **DS2155, DS21Q55**, and **DS2156** do **NOT** require any special initialization whatsoever since they automatically initialize upon power-up. It is a good idea to clear—set to 0x00—**ALL** R/W registers. The easiest way to do this is to write 0x00 to address space 0x00–0xFF, regardless of register type. Certain registers have bits that control special test modes and features that can provide confusing indications (Table 1).

Table 1. Registers with Special Test Modes and Features

PART	NAME	PART	NAME
DS2151	TEST, TCR2, LICR	DS2153	TEST1, TEST2, LICR
DS2152	TEST1, TEST2, TCR2, LICR	DS2154	TEST1, TEST2, LICR
DS21352/552	TEST1, TEST2, TCR2, LICR	DS21354/554	TEST1, TEST2, TCR2, LICR
DS21Q41/Q42	TEST, TCR2	DS21Q43/Q44	TEST1, TEST2
DS21FF/FT42	TEST1, TCR2	DS21FF/FT44	TEST1, TEST2

Depending on the interrupt structure implemented, it may be a good idea to clear IMR1 and IMR2 first. Prior to clearing these two registers, spurious interrupt signals may occur without an external interrupt disable.

Once the registers have been initialized and set up with the transceiver's mode of operation, the line interface reset bit should be set high, then low. If the elastic store is enabled, the ESR bit should be set, then cleared.

SPECIAL INITIALIZATION FOR DS2141

Transmit clock (TCLK) must be present for proper port initialization. Network signals (loop timing) cannot be guaranteed to replace a missing TCLK during initialization. The following sequence should be used to initialize the **DS2141**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for SYSCLK to stabilize if elastic stores enabled

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SPECIAL INITIALIZATION FOR DS21Q41

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the **DS21Q41**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **TCR1** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
- Set **ESR** bit in **CCR3** register if elastic stores enabled
- Clear **ESR** bit.

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in **TCR1** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS21Q42

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the **DS21Q42**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **TCR1** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
- Set **TESR** and **RESR** bits in **CCR7** register if elastic stores enabled
- Clear **TESR** and **RESR** bits.

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in **TCR1** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS2143

Transmit clock (TCLK) must be present for proper port initialization. Network signals (loop timing) cannot be guaranteed to replace a missing TCLK during initialization. The following sequence should be used to initialize the **DS2143**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for SYSCLK to stabilize if elastic stores enabled

SPECIAL INITIALIZATION FOR DS21Q43

Transmit Clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK via the LOSS of TRANSMIT CLOCK mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the **DS21Q43** in which TCLK is not present or TCLK is derived from RCLK (a loop timed system).

- Set **LOTCMC** bit in **CCR2** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for TSYSCLK and RSYSCLK to stabilize (if elastic store(s) enabled)
- Set **ESR** bit in **CCR3** register (if elastic store(s) enabled)
- Clear **ESR** bit

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in C**CR2** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS21Q44

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the **DS21Q44**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **CCR2** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for TSYSCLK and RSYSCLK to stabilize (if elastic store(s) enabled)
- Set **TESR** and **RESR** bits in **CCR6** register (if elastic store(s) enabled)
- Clear **TESR** and **RESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in C**CR2** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS2151

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the **DS2151**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **TCR1** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- SET **LIRST** bit in **CCR3** register
- Wait for SYSCLK to stabilize if elastic stores enabled
- Set **ESR** bit in **CCR3** register if elastic stores enabled
- Clear **LIRST** and **ESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in T**CR1** be enabled.
Note 2: If the SYSCLK pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS2152

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the **DS2152**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **TCR1** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Set **LIRST** bit in **CCR7** register
- Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
- Set **ESR** bit in **CCR3** register if elastic stores enabled
- Clear **LIRST** and **ESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in T**CR1** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS2153

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the **DS2153**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **CCR2** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Set **LIRST** bit in **CCR3** register
- Wait for SYSCLK to stabilize (if elastic store(s) enabled)
- Set **ESR** bit in **CCR3** register (if elastic store(s) enabled)
- Clear **LIRST** and **ESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in C**CR2** be enabled.
Note 2: If the SYSCLK pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS2154

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the **DS2154**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **CCR2** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Set **LIRST** bit in **CCR5** register
- Wait for TSYSCLK and RSYSCLK to stabilize (if elastic store(s) enabled)
- Set **ESR** bit in **CCR3** register (if elastic store(s) enabled)
- Clear **LIRST** and **ESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in C**CR2** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS21FF/FT42

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the **DS21FF/FT42**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **TCR1** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for SYSCLK to stabilize if elastic stores enabled
- Set **TESR** and **RESR** bits in **CCR7** register if elastic stores enabled
- Clear **TESR** and **RESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in T**CR1** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS21FF/FT44

Transmit Clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the **DS21FF/FT44**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **CCR2** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Wait for SYSCLK to stabilize if elastic stores enabled
- Set **TESR** and **RESR** bits in **CCR6** register if elastic stores enabled
- Clear **TESR** and **RESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in C**CR2** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS21x52

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the **DS21x52**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **TCR1** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Set **LIRST** bit in **CCR7** register
- Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
- Set **TESR** and **RESR** bits in **CCR7** register high if elastic stores enabled
- Clear **LIRST**, **TESR**, and **RESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in T**CR1** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

SPECIAL INITIALIZATION FOR DS21x54

Transmit Clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the **DS21x54**, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

- Set **LOTCMC** bit in **CCR2** register
- Wait 10ms minimum
- Write 0x00 to all other R/W registers
- Write initial device configuration data
- Set **LIRST** bit in **CCR5** register
- Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
- Set **TESR** and **RESR** bits in **CCR6** register high if elastic stores enabled
- Clear **LIRST**, **TESR**, and **RESR** bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that **LOTCMC** in C**CR2** be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

CONCLUSION

If you have further questions about T1/E1 framer initialization and programming, please contact the Telecommunication Applications support team via email telecom.support@dalsemi.com or call (972) 371 - 6555.

T1/E1 FRAMER INFORMATION

For more information about our T1/E1 framers, please consult the respective data sheets available on our website at www.maxim-ic.com/telecom.